REMARKS

The foregoing amendments are to more particularly point out the claimed subject matter rather than to avoid the prior art.

Applicant respectfully requests reconsideration of the above identified application. Claims 16, 18, 21-24 and 39-44 are pending. Claims 16, 18, 21-22, 39-41 and 43-44 are rejected. Claims 23 and 24 are allowed. Claim 42 is objected to. Claims 16 and 39 are amended.

The Office Action mailed on April 9, 2008, rejects claim 16 under 35 USC 102(e) as allegedly being anticipated by US Patent 5,996,066 (Yung).

Applicant respectfully submits that claim 16, as currently amended, is not anticipated by Yung.

The Examiner indicates that the "pixel distance" of Yung (col. 5 lines 25-27) would be interpreted as the packed sum of absolute differences (PSAD) instruction and that the "single instruction [that] does both a multiply of two partitioned values, and an add with a separate, third value, with a masking capability," (col. 2 lines 10-14) would be interpreted as the packed multiply-add (PMAD) instruction.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Applicant has respectfully argued that one skilled in the art would distinguish at least between the multiply-accumulate with masking instruction of Yung and the claimed PMAD instruction. As Applicant has pointed out, Yung distinguishes between them (e.g. col. 6, line 51-53) saying that, "The result of the multiplication is added in an adder/subtractor 96 with a value from a register 98 (as opposed to adding together partitioned fields of the multiply result as done in the Intel MMX instruction)." (i.e. PMAD).

Claim 16 as amended, clearly points out that the second set of operations for the PMAD instruction include multiplying corresponding packed data elements of the second set of packed data to produce products and summing said products by pairs.

Applicant further submits that Yung does not disclose enough to anticipate the PSAD instruction, but if one skilled in the art is presumed to understand the vis_pdist instruction of Sun Microsystems, Inc., then one skilled in the art would also distinguish between it and the claimed PSAD instruction.

Therefore, Applicant respectfully submits that claim 16, as amended, is not anticipated by Yung.

The Office Action further rejects claim 16 and also rejects claim 18 under 35 USC 103 as allegedly being unpatentable over Yung in view of US Patent 5,734,874 (Van Hook) and rejects claims 21-22 under 35 USC 103 as allegedly being unpatentable over Yung in view of Van Hook and further in view of US Patent 5,721,697 (Lee).

Applicant respectfully submits that at least in light of the above arguments, one skilled in the art would distinguish the second set of operations for the PMAD instruction as set forth by claim 16, as amended, from the disclosure of Yung.

The disclosures of Van Hook and Lee are insufficient to remedy the problems of Yung. Therefore, Applicant respectfully submits that claim 16, 18, and 21-22 are not obvious from the cited references.

The Office Action rejects claims 39-41 under 35 USC 102(e) as allegedly being anticipated by Van Hook.

Applicant respectfully submits that claim 39 as amended, clearly points out decode logic to generate a microcode sequence responsive to decoding the PSAD instruction to initiate a first set of operations on the first set of packed data.

Van Hook discloses (col. 5, lines 11-17) that "At each dispatch, the PDU 46 may dispatch either a pixel distance computation instruction, a graphics data partitioned multiplication instruction, a graphics data packing instruction, or a graphics data compare instruction to the second partitioned execution path 34. The pixel distance computation circuit 56 executes the pixel distance computation instruction."

Thus one skilled in the art would determine that the PDU 46 does not anticipate the claimed decode logic to generate a microcode sequence responsive to decoding the

PSAD instruction to initiate the three claimed operations, but simply dispatches the PDIST instruction of Van Hook.

Two prior techniques for computing an absolute differences found in the design of floating point mantissa arithmetic are: (1) compare two numbers and reorder to subtract the smaller from the larger, or (2) subtract the two numbers in both directions and select the positive result. Applicant respectfully submits that in the context of the entire patent including the specification, one skilled in the art would distinguish between the two techniques listed above and the claimed packed subtract and write carry (PSUBWC) operation and the packed absolute value and read carry (PABSRC) operation set forth by the present application.

Van Hook discloses (col. 10, line 65 through col. 11, line 9) that, "As shown in FIG. 9b, in this embodiment, the pixel distance computation circuit 56 comprises eight pairs of 8 bit subtractors 57a-57h. Additionally, the pixel distance computation circuit 56 further comprises three 4:2 carry save adders 61a-61c, a 3:2 carry save adder 62, two registers 63a-63b, and a 11-bit carry propagate adder 65, coupled to each other as shown. The eight pairs of 8 bit subtractors 57a-57h, the three 4:2 carry save adders 61a-61c, the 3:2 carry save adder 62, the two registers 63a-63b, and the 11-bit carry propagate adder 65, cooperate to compute the absolute differences between eight pairs of 8-bit values, and aggregate the absolute differences into a 64-bit sum."

Thus from Fig. 9b of Van Hook and the above disclosure, one of skill in the art may conclude that Van Hook performs the second known technique (2) rather than the claimed microcode sequence to initiate the PSUBWC operation and the PABSRC operations.

Therefore, Applicant respectfully submits that claims 39-41, as currently amended, are not anticipated by the cited reference.

The Office Action rejects claims 43-44 under 35 USC 103 as allegedly being unpatentable over Van Hook in view of Lee.

Applicant respectfully submits that the disclosure of Lee is insufficient to remedy the problems of Van Hook with regard to claim 39. Moreover, Van Hook discloses (col. 5, lines 16-19) that the pixel distance computation circuit 56 executes the pixel distance

computation instruction, but partitioned multiplier 58 executes the graphics data partitioned multiplication instructions.

Thus without a suggestion to modify Van Hook, it must be assumed that the combination results from impermissible hindsight using Applicant's own disclosure. Applicant respectfully notes that such a modification of Van Hook is not at all obvious and is lacking an expectation of success. For example, note the 11-bit carry propagate adder 65 and the 53-bit increment 63a of Figure 9b, which may satisfy a critical timing constraint in Van Hook and are not be found in Lee. Therefore, Applicant respectfully submits that claims 43-44 are not obvious from the cited references.

CONCLUSION

Applicant respectfully submits the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due.

Respectfully submitted,

Date: July 3, 2008

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